REMARKS

The Examiner is thanked for the interview courteously granted to the undersigned, in connection with the above-identified application. During this interview, an amended claim 103 was presented to the Examiner for his consideration, and at the interview differences between this amended claim 103 and the references applied by the Examiner in the Office Action mailed December 1, 2004, were discussed. In addition, advantages achieved by the present invention were discussed; and it was pointed out to the Examiner, consistent with arguments made in previous amendments, that evidence in applicants' disclosure (in particular, in Figs. 9-14) showed unexpectedly better results achieved according to the present invention, wherein the top of the semiconductor substrate and the top of the conductive film (gate electrode) were removed to 2.5 nm or less below the respective surfaces of the semiconductor substrate and of the conductive film (gate electrode), by sputter-etching. No agreement was reached during the interview.

Applicants have amended the claims consistent with amendments to claim 103 as discussed during the aforementioned interview, and in order to further clarify various aspects of the present invention. Specifically, claims 103, 124 and 127 have been amended to recite a step of forming an isolating element in a semiconductor substrate; to recite that the conductive film or gate electrode is formed on the gate insulating film and on the isolating element; and to recite removal of the top of the conductive film or gate electrode by 2.5 nm or less below the surface of the conductive film or gate electrode, by sputter-etching. In light of these amendments to claims 103, 124 and 127, claims 111, 122, 123 and 131 have been canceled

without prejudice or disclaimer, and dependencies of various of the other previously considered claims have been amended.

In addition, applicants are adding new claims 133-144 to the application. Claims 133-135, dependent respectively on claims 103, 124 and 127, recite that the step (a) of forming the isolating element in the semiconductor substrate includes forming a trench in the semiconductor substrate, and depositing an insulating film in the trench. Claims 136-138, dependent respectively on claims 103, 124 and 127, recite that by the step of removing the top of the semiconductor substrate and the top of the conductive film (gate electrode) by sputter-etching, a height of steps of the conductive film (gate electrode) formed over the semiconductor substrate and over the isolating element is reduced. Claims 139, 141 and 143, dependent respectively on claims 103, 124 and 127, recite that a step is formed at an end of the isolating element, and a corresponding step is carried over to the conductive film formed on the step formed at the end of the isolating element; and claims 140, 142 and 144, dependent respectively on claims 139, 141 and 143, recite that in removing the top of the conductive film (gate electrode), a height of the corresponding step is reduced.

In connection with the presently submitted claims, note, e.g., Fig. 17 and the corresponding description in connection therewith in paragraph [0069] on page 26 of applicants' Substitute Specification submitted with the Preliminary Amendment filed November 27, 2001.

Applicants respectfully submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the documents applied by the Examiner in rejecting claims in the Office Action mailed

December 1, 2004, that is, the teachings of the U.S. Patents to Zeininger et al, No. 5,344,793, and to Kamal et al, No. 6,303,503, European Patent Application No. 325328, and the publications of Hong et al, "$CoSi_2$ With Low Diode Leakage and Low Sheet Resistance At 0.065 μm Gate Length, in IEDM 97, pages 107-110, Lee et al, "A High Performance 0.13 μm CMOS Process for ghz Microprocessor Manufacture" in IEEE 6th International Conference of VLSI and CAD (October 1999), pages 136-139, Yan et al "High Performance 0.1-μm Room Temperature Si MOSFETs", in 1992 Symposium on VLSI Technology Digest of Technical Papers (1992), pages 86 and 87, and Rho et al, Dependence of Deep Submicron CMOSFET Characteristics on Shallow Source/Drain Junction Depth", in International Conference of Microelectronics and VLSI (1995), pages 291-294, under the provisions of 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, including forming a respective isolating element and gate insulating film on a semiconductor substrate, and forming a conductive film (gate electrode) on the insulating film and isolating element, the conductive film having a width of 0.18 μm or less; and removing the top of the semiconductor substrate and removing the top of the conductive film (gate electrode) to 2.5 nm or less below the surface of the semiconductor substrate and conductive film (gate electrode) respectively, by sputter-etching, with silicide layers being formed in the surface of semiconductor region (source/drain regions) and the conductive film (gate electrode). See claim 103; note also claims 124 and 127.

Furthermore, it is respectfully submitted that these references would have neither taught nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claim, having features as discussed previously in connection with independent claims 103, 124 and 127, and, moreover, wherein in removing, *inter alia*, a top surface of the conductive film (gate electrode), a height of steps of the conductive film (gate electrode) formed over the semiconductor substrate and over the isolation element is reduced (see claims 136-138); and/or wherein a step is formed at an end of the isolating element, with a corresponding step being carried over to the conductive film (gate electrode) formed on the step formed at the end of the isolating element (see claims 139, 141 and 143), and wherein in removing the top of the conductive film (gate electrode) a height of this corresponding step carried over to the conductive film is reduced (see claims 140, 142 and 144).

Furthermore, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a method of fabricating a semiconductor integrated circuit device as in the present claims, having features as discussed previously in connection with claims 103, 124 and 127, and, moreover, having additional features as in the remaining dependent claims, including (but not limited to) wherein the isolating region is formed by forming a trench in the semiconductor substrate and depositing an insulating film in the trench (see claims 133-135); and/or wherein the sputter-etching is carried out after the surface of the semiconductor substrate and the conductive film have been cleaned by using hydrofluoric acid as a cleaning agent (see claim 107); and/or wherein the sputter-etching is Ar sputter-etching (see claims 108 and 128); and/or wherein the

silicide layers are cobalt silicide layers (see claims 109 and 129), particularly having a thickness as in claims 110 and 130; and/or wherein the top of the conductive film (gate electrode) is sputter-etched simultaneously with the sputter-etching away the top of the semiconductor substrate (see claims 112 and 132).

Furthermore, and as will be discussed further, infra, it is respectfully submitted that even assuming, *arguendo*, that the teachings of the applied prior art would have established a *prima facie* case of obviousness, the evidence in applicants' disclosure shows unexpectedly better results achieved according to the present invention in sputter-etching at most 2.5 nm below the surface of the semiconductor substrate/conductive film (gate electrode), overcoming any such *prima facie* case of obviousness and supporting unobviousness of the presently claimed subject matter. This evidence in applicants' disclosure must be considered in any determination of obviousness. See In re DeBlauwe, 222 USPQ 191 (CAFC 1984).

As for this evidence of unexpectedly better results, attention is respectfully directed to Fig. 9 and the description in connection therewith in paragraphs [0049]-[0051] on pages 20 and 21 of applicants' Substitute Specification, together with Figs. 10-13 and the description in connection therewith in paragraphs [0054]-[0056] on pages 21-23 of this Substitute Specification. It is respectfully submitted that this evidence shows unexpectedly better results achieved according to the present invention, wherein the sputter-etching etches away only 2.5 nm or less below the surface of the semiconductor substrate and below the surface of the conductive film (gate electrode), overcomes any *prima facie* case of obviousness, and clearly supports patentability of the presently claimed subject matter.

Thus, Fig. 9 is a graph showing a first set of data to indicate a relationship between the amount of sputter-etching and the yield of products. As shown in line (a) of Fig. 9, a yield of approximately 90 % can be ensured by an amount of sputter-etching from among 0, 1, 2, 3 or 4 nm when the critical value of the standby current (Isb) is set to 28 μm or less. However, when the critical value of the standby current (Isb) is set to 5 μA or less as shown in line (b), the yield is improved when the amount of sputter-etching is 1 or 2 nm, as compared with the case where no sputter-etching is carried out (that is, the amount of sputter-etching is 0). Moreover, when the amount of sputter-etching 3 or 4 nm, the yield becomes lower than in the case where no sputter-etching is carried out; the yield dropped to approximately 0 when the amount of sputter-etching was 4 nm. As is clear from Fig. 9, a semiconductor integrated circuit device for which the amount of sputter-etching is 3 nm or above cannot be adopted for use in products featuring a low consumption of current that have a critical value for standby current (Isb) of 5 μA or less.

As seen in the foregoing paragraph, the amount of sputter-etching according to the present invention provides unexpectedly better results, in being adaptable for use in products featuring a low consumption of current that have a critical value for standby current (Isb) of 5 μA or less.

In addition, attention is respectfully directed to a second set of data shown in Figs. 10-13 and described in paragraphs [0054] - [0056] on pages 21-23 of applicants' Substitute Specification. These figures show that when no sputter-etching is carried out (the amount of sputter-etching being 0), there are 197 chips with standby current flows of 3.5-4 μA, as seen in Fig. 10. As depicted in Figs. 11 and 12, when the amount of sputter-etching is 1 nm and 2 nm, respectively, there

are 496 chips with standby current flows of 2.5 to 3 μA, and 479 chips with standby current flows of 4 μA or less. As seen in Fig. 13, when the amount of sputter-etching is 3 nm, there are 202 good chips with standby current of 4-4.5 μA. As can be appreciated, the smaller the standby current, the better the performance of a chip; consequently, when the amount of sputter-etching is set to 2.5 nm or less, more chips with lower level of standby current can be obtained, hence more chips with high-levels of performance can be obtained.

It is respectfully submitted, that this evidence shows unexpectedly better results in lower levels of standby current, with higher levels of performance, obtained according to the present invention, as compared with, for example, sputter-etching at levels greater than that in the present claims or with no sputter-etching.

It is further respectfully submitted that by reducing the standby current of the semiconductor integrated circuit device, consumption of current is reduced. As a result, semiconductor integrated circuit devices formed by the present method are applicable in cellular phones and personal computers which are battery-driven, as they are able to lengthen the times over which these products are used.

Attention is also directed to Fig. 15 of the above-identified application, and the description in connection therewith in paragraph [0064] on pages 25 and 26 of applicants' Substitute Specification. As is clear therefrom, when the sputter-etching is undesirably great, for example, greater than 2.5 nm, upon forming the silicide the metal silicide layer approaches the junctions of the source/drain regions, increasing the current leakage. This is avoided according to the present invention; having the sputter-etching to a depth of at most 2.5 nm, such approach to the junction, and resulting increase in the leakage current, can be avoided.

In addition, by etching the surface of the gate electrode by a relatively small thickness (2.5 nm or less), a discontinuity of the layer of metallic silicide can be avoided, so that increase of resistance of the gate electrode layer and a resulting decrease in operation speed, can be avoided. Note paragraphs [0067]-[0069] on pages 26-28 of the applicants' Substitute Specification. Moreover, with simultaneous etching of the top of the substrate and the top of the gate electrode, as in various of the present claims (see, e.g., claims 112, 123 and 132), processing is facilitated and simplified.

European Patent Application No. 325,328 discloses a method of manufacturing a semiconductor device, which includes providing a substrate having doped semiconductor regions for forming at least one electrical component, at least one of the doped regions having an exposed surface area, and depositing metal for forming a metal silicide at the exposed area, with the exposed surface area being subjected to sputter-etching prior to depositing the metal to form the metal silicide. This patent document goes on to disclose that the sputter-etching enables oxide to be removed which would, despite conventional chemical wet etching to remove native oxide during previous processing steps, form on the exposed silicon surface area, and that removal of this oxide facilitates formation of the subsequent silicide. Note column 2, lines 4-22. This patent document also discloses that the sputter-etching also forms a layer of amorphous silicon at each exposed silicon surface area; and thus not only does the sputtering remove oxide which can be detrimental to silicide formation, but the disclosed method also provides silicon having the same or at least a similar physical structure at each exposed surface area. See column 3, lines 2-10. Note also, column 3, lines 23-26, disclosing ions of an inert gas,

preferably argon, being used to sputter-etch the exposed surface areas. Note also from column 6, line 48 to column 7, line 8; column 7, lines 12-16, 26-33 and 39-46; and column 8, lines 7-12. As a specific example, this patent document discloses in the paragraph bridging columns 7 and 8, that argon sputter-etching is performed to remove from the substrate a thickness of silicon oxide of the order of 10 nm while providing specified amounts of amorphous silicon, and with argon contamination to a depth within the substrate of less than 20 nm, probably in the region of between 5 and 10 nm. This patent discloses sputter-depositing a layer of refractory metal, of approximately 30-100 nm in thickness. See column 8, lines 12-16. Note also column 9, lines 32-50, emphasizing that the sputter-etching provides an amorphous silicon surface at each exposed surface area so that the metal (e.g., titanium) deposited, is deposited onto the same given type of silicon at each exposed surface, regardless of the type of silicon.

Initially, it is emphasized that according to the method in No. 325,328, the silicon material surface is formed into an amorphous surface. It is respectfully submitted that this disclosure would have neither taught nor would have suggested, and in fact would have taught away from, removing the top of the semiconductor substrate to 2.5 nm or less below the surface of the semiconductor substrate by sputter-etching, as in the present invention, and advantages thereof. It is respectfully suggested that by expressly disclosing formation of an amorphous surface, this would have taught away from removing the substrate surface, by sputter-etching, to the depth as in the present claims.

It is emphasized that No. 325,328 discloses a contamination depth of argon of less than 20 nm, probably in the region of between 5 and 10 nm. Clearly, this

disclosure of a contamination depth would have neither taught nor would have suggested the removing as in the present claims, much less such removing to a depth of 2.5 nm or less, and advantages thereof as established by the evidence of record.

Furthermore, it is respectfully submitted that the applied European Patent Application provides a general disclosure with respect to use of sputter-etching in formation of a metal silicide. It is respectfully submitted that this reference does not disclose, nor would have suggested, such a fabrication method as in the present claims, including forming the isolating element in the semiconductor substrate, particularly the step formed at the end of the isolating element, and problems arising in connection with this step, as discussed previously; and would have neither taught nor would have suggested the additional processing according to the present invention of removing, *inter alia*, the top of the conductive film (gate electrode) to 2.5 nm or less by sputter-etching, and reducing the steps. Note, especially, claims 136-144.

The contention by the Examiner in the paragraph bridging pages 3 and 4 of the Office Action mailed December 1, 2004, that No. 325,328 discloses, *inter alia*, argon sputter etching of less than 20 nm, thus encompassing less than 2.5 nm, is noted. The Examiner is respectfully challenged to point out the specific description in the applied European Patent Appln. for argon sputter-etching for removal of the substrate of less than 20 nm. While this applied European Patent Application discloses argon contamination to a depth within the monocrystalline silicon substrate of less than 20 nm, probably in the region of between 5 and 10 nm, in the paragraph bridging columns 7 and 8 thereof, it is respectfully submitted that such disclosure

does not teach, nor would have suggested, argon sputter-etching for removing the substrate of less than 20 nm.

Additionally, it is again emphasized that applicants have shown unexpectedly better results achieved through use of the removal, by sputter-etching, of 2.5 nm or less from the top of the semiconductor substrate. Even assuming, *arguendo*, that the applied European Patent Application disclosed argon sputter-etching of "less than 20 nm", as alleged by the Examiner, such disclosure would not have taught the unexpectedly better results achieved at removal levels of 2.5 nm or less particularly in view of the disclosure in the applied European Patent Application of argon contamination "of less than 20 nm, probably in the region of between 5 and 10 nm".

Furthermore, the applied European Patent Application is concerned with sputter-etching the semiconductor substrate. Such disclosure would have neither taught nor would have suggested the removing of the conductive film (gate electrode), to a depth of 2.5 nm or less from the surface thereof, or the unexpectedly better results in avoiding discontinuities at steps of the conductive film, as discussed previously.

It is respectfully submitted that the secondary references as applied by the Examiner would not have rectified the deficiencies of the applied European Patent Application such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Zeininger et al discloses defect-enhanced $CoSi_2$ formation and improved silicided junctions in deep submicron MOSFET. According to an aspect described in this patent, a silicon wafer is first pre-cleaned with hydrofluoric acid. After the HF precleaning, the silicon wafer is transferred to a conventional cobalt sputtering tool

where it is sputter-cleaned by bombardment with low energy ions. After the sputter cleaning, cobalt metal is deposited on the silicon wafer at room temperature so as to form the $CoSi_2$ layer. Note the paragraph bridging columns 1 and 2 of this patent; see also column 2, lines 39-42 and 58-64.

Kamal et al discloses processes for the formation of cobalt silicide layers during semiconductor device fabrication, including a sputter etch surface preparation step prior to the cobalt layer deposition step. The sputter etch is described as an argon sputter etch with a DC bias of less than -280 volts, the argon sputter etch process conditions being optimized in order to minimize backsputtering of silicon onto the gate side wall spacers, while still adequately removing native silicon dioxide from the source region, drain region and silicon gate. See column 2, lines 48-66. Note also column 3, lines 9-11; and column 5, lines 60-65.

Hong et al reports on an investigation of effectiveness of four methods for diode leakage reduction and their impact on sub-0.18μm CMOS device performance. This article discloses that key results show (1) pre-Co deposition sputter clean can reduce leakage but only to a certain extent; (2) ion amorphization tightens diode leakage distribution at a cost of increasing source-to-drain series resistance and its extendibility to shallower junctions is questionable; (3) high temperature silicidation significantly improves diode leakage but increases source-to-drain series resistance; and (4) high temperature Co deposition can improve diode leakage even at low RTP temperatures. Note the paragraph bridging the left-and right-hand columns on page 107. See also the first full paragraph in the right- hand column on page 107.

Lee et al proposes a highly manufacturable and high performance 0.13 μm CMOS technology to meet the requirements for future gigaherz microprocessor

application. The technology includes shallow trench isolation, aggressive doping engineering for threshold adjustment and gate doping, dual gate CMOS transistors, and advanced Co-salicide for low resistance.

Even assuming, *arguendo*, that the teachings of the references applied against claims 103 and 105-116 were properly combinable, the combined teachings of these references would have neither disclosed nor would have suggested the presently claimed method including formation of the isolating element and problems arising in connection therewith, particularly with respect to steps at ends thereof (note especially claims 136-144); and/or removing 2.5 nm or less from both the semiconductor substrate and the conductive film (gate electrode) by sputter-etching, and advantages thereof, particularly with respect to structure having the steps at ends of the isolating element; and/or other advantages of the present invention as discussed in the foregoing.

It is respectfully submitted that, clearly, the teachings of the applied prior art would have neither disclosed nor would have suggested the unexpectedly better results achieved according to the present invention, through removal of 2.5 nm or less of the semiconductor substrate and/or conductive film (gate electrode).

In the paragraph bridging pages 5 and 6 of the Office Action mailed December 1, 2004, the Examiner contends that the removal of 2.5 nm or less of the top of the semiconductor substrate would have been met in the applied European Patent Application or Hong. As discussed previously, applicants found no disclosure in the applied European Patent Application of removal of the semiconductor substrate to a depth of 20 nm or less, and the Examiner is respectfully requested to point out the specific disclosure in the applied European Patent Application of such

removing. Moreover, it is respectfully submitted, that Hong, et al, discloses generally a short time Ar/H_2 sputter clean; the Examiner is respectfully challenged to point out the specific disclosure in Hong of removal of 2.5. nm or less of the top of the semiconductor substrate.

Furthermore, the Examiner has not even alleged a removal of an amount from the top surface of the conductor film/gate electrode as in all of the claims presently being considered on the merits, and as in previously considered claim 111, 122 and 131, for example. It is respectfully submitted that the applied references would have neither taught nor would have suggested such removal of the conductive film (gate electrode) as in the present claims and advantages thereof as discussed in the foregoing.

In connection with previously considered claims 117-132, the article by Rho et al discloses a new technique named MOSES (Mask Oxide Sidewall Etch Scheme) for fine gate patterning of 0.1 μm dimensions. See the first full paragraph in the right-hand column on page 291,and the paragraph bridging pages 291 and 292). It is disclosed that optimized channel implants are performed with the concept of vertical doping engineering, after conventional well and LOCOS isolation processing.

Yan et al discloses the design and implementation of 0.15 μm channel N-MOSFETs with very high current drive and good short channel behavior at room temperature. The MOSFETs were fabricated using e-beam lithography for gate definition and self-aligned $TiSi_2$ silicides to reduce parasitic resistances. See the paragraph bridging the left- and right-hand columns on page 86 of this article.

Even assuming, *arguendo*, that the teachings of Rho et al or Yan et al were properly combinable with the other documents as applied by the Examiner, it is

respectfully submitted that the combined teachings of these documents would have neither disclosed nor would have suggested the presently claimed process, including formation of the isolating element and problems arising in connection with the present structure formed including the isolating element, and particularly including the steps as in various of the present claims; and avoiding such problems utilizing the removal by sputter-etching of the top surface of the substrate and conductive film (gate electrode) of the maximum depth as in the present claims and, in particular, the unexpectedly better results achieved by the maximum removal of the substrate as in the present claims and/or the maximum removal of the conductive film (gate electrode) and advantages thereof; and/or the other features of the present invention, and advantages thereof, as discussed previously.

Again, applicants refer to the unexpectedly better results achieved according to the present invention, as seen from the evidence of record. Particularly in view thereof, it is respectfully submitted, that the teachings of the applied documents would have neither disclosed nor would have suggested the presently claimed invention, under the requirements of 35 USC §102 and 35 USC §103.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by a personal interview, the Examiner is invited to contact the undersigned representative at the number indicated below.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.40724X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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